HalfGRAPH2 – A digitizer ASIC for Space Applications

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TECHNE INSTRUMENTS
Hardware & Instrumentation Design

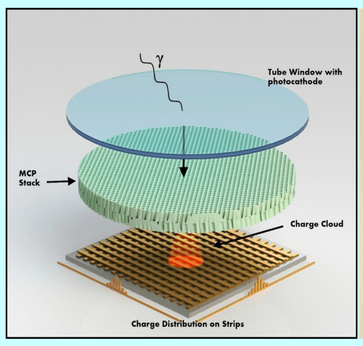
1. Motivation:

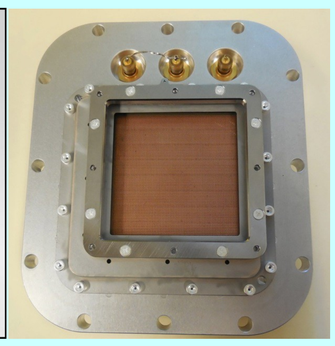
Space Sciences Laboratory (SSL) – UC Berkley developed a spatially sensitive 2D ultraviolet (UV) single-photon counting detector for space applications based on a microchannel plate (MCP). NASA Strategic Astrophysics Technology (SAT) program has funded an upgrade to the detector.

Upgrade requirements:

- Upgrade and minimize the readout electronic system
- Lower the system power consumption
- Increase event rate > 1Mhz/channel
- Enable low noise measurements (1000e-)
- Improve NASA Technology Readiness Level from 4 to 6

-> We designed application specific chips.





Detector construction:

-UV sensitive CsI photo cathode (100-200nm)
-MCP stack
-Cross strip array
-Spatial resolution ~20um, 2Mhz event/rate

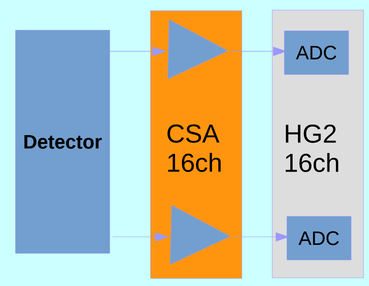
Cross strip anode readouts for large format, photon counting microchannel plate detectors : developing flight qualified prototypes of the detector and electronics.
Conference: Space Telescopes and Instrumentation 2014 : ultraviolet to gamma ray., At Montréal, Canada, Volume: Proceedings of SPIE

2. Detector Readout System

- Deposited charge per single photon ~160fC

- Charge to voltage conversion by programmable amplifier
  See: CSAv3- a Charge Sensitive Amplifier for Space Applications –> N2AP-53 poster.

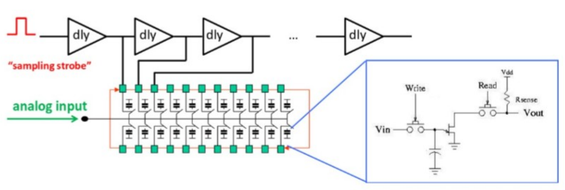
- High speed digitizer –> **HalfGraph2**



3. Digitizer specifications:

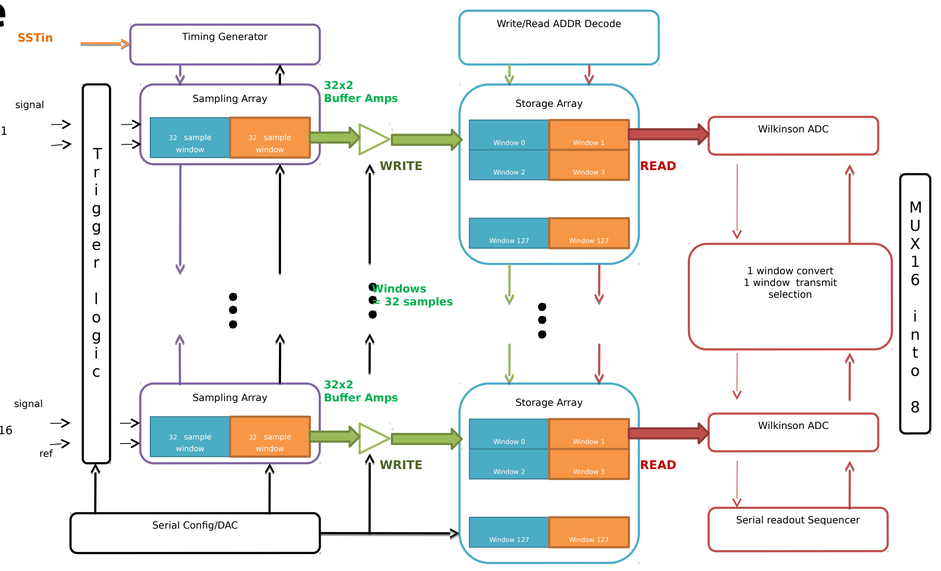
- 16 input channels
- 1 GSPS / channel
- 12bit resolution
- 8us memory / channel
- Small package

4. Sampling window



5. ASIC architecture

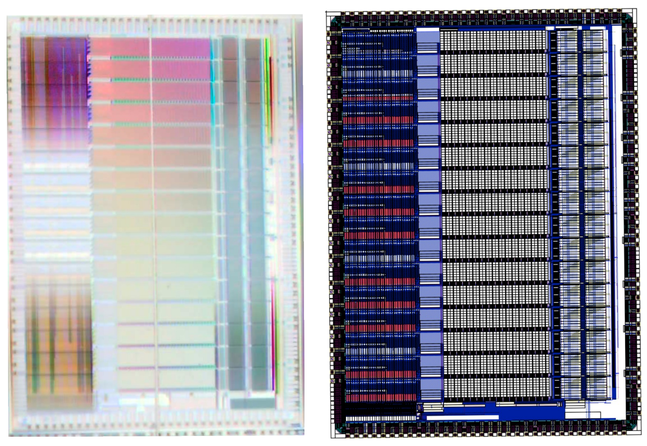
- Serial shift register for slow control
- Programmable trigger logic
- Sampling windows
- Storage windows
- 128 memory windows of 64 cells → 8us/channel
- Wilkinson converters
- Routing multiplexer for data output streams.
- 8 ch LVDS serial data output



6. Operation

- An FPGA is required to control the chip.
- The sampling base runs continuously.
- Two sampling windows (32 samples each) are transferred into storage array in a ping/pong fashion given a write location.
- Triggers are threshold programmable.
- When trigger strobes, a location in memory is converted using internal Wilkinson converters.
- The chip allows to convert and transmit data simultaneously.
- An multiplexed output connects serial data outputs to 8 consecutive channels of interest.

7. Layout



- TSMC 250nm technology
- LQFP 128 pin package

8. Target performance

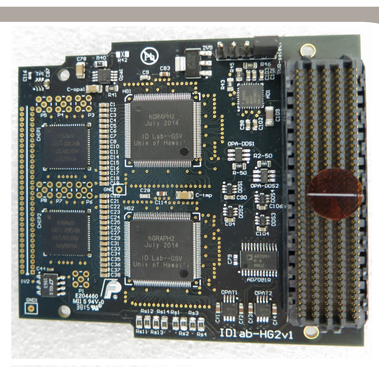
Readout time estimation per event

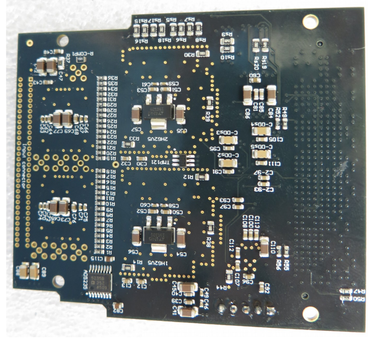
- Expected pulse with FWHM of 50ns.
- This corresponds to ~64 samples (12bit each) matches ~ 800bit of data/ event.
- At 500MHz shift clock → **~1.5us/event**
  We read 8 channels in parallel.
- Possible continuous event rate/channel
  → 5.2M events/s/channel.
- Possible improvement with more selective triggering and shorter amplifier shaping times.

9. Pre-prototype readout system

- 32 channel front end system (amps and digitizers)
- "FMC" form factor designed for ML605*
- Allows setting remotely all of the necessary parameters
- On board signal test generators for amplifiers and digitizers
- Remote health monitoring (power rails,basline voltages,etc)
-Unified Giga bit Ethernet connection to computer.

*ML605 – Xilinx evaluation board.





10. Future work

- System performance evaluation.
- FPGA algorithm optimization for particular detector.
- Operation in radiation exposure.
- High voltage spark vulnerability.
- Prepare a prototype for detector tests.